	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	525	program with (runway or run adj2 away)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	2006/03/02 07:46
2	BRS	L2	42	(program with (runway or run adj2 away)).clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	2006/03/02 08:17

	Comments	Error Definition	Errors
1			
2			

	Type	L #	Hits	Search Text	DBs	Time Stamp
12	BRS	L12	1	((counter adj3 reset or cr) same (wdt or watch adj5 timer)).clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	2006/03/02 08:36
13	BRS	L13	6	((counter adj3 reset or cr) same (wdt or watch adj5 timer) same (program$4 or instruction or execu$4)).ab.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	2006/03/02 08:37
14	BRS	L15	0	("2004/0037156").URPN.	USPAT	2006/03/02 08:38
15	BRS	L14	25	((counter adj3 reset or cr) same (wdt or watch adj5 timer) same (program$4 or instruction or execu$4))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	2006/03/02 08:49

	Comments	Error Definition	Errors
12			
13			
14			
15			

	Type	L #	Hits	Search Text	DBs	Time Stamp
16	BRS	L16	2	((counter adj3 reset or cr) same (wdt or watch adj5 timer) same (program$4 or instruction or execu$4) same (backup or backing adj3 up))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	2006/03/02 08:50
17	BRS	L17	1356	711/162.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	2006/03/02 09:06
18	BRS	L18	0	1 and 17	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	2006/03/02 09:06

	Comments	Error Definition	Errors
16			
17			
18			

PAT-NO: JP411212829A

DOCUMENT-IDENTIFIER: JP 11212829 A

TITLE: METHOD AND SYSTEM FOR WDT MONITORING

PUBN-DATE: August 6, 1999

INVENTOR-INFORMATION:

NAME	COUNTRY
YAMAMOTO, KYOKO	N/A
MACHIDA, TAKASHI	N/A
KAWAMICHI, MAKOTO	N/A

ASSIGNEE-INFORMATION:

NAME	COUNTRY
NEC CORP	N/A
NEC TELECOM SYST LTD	N/A

APPL-NO: JP10026527

APPL-DATE: January 23, 1998

INT-CL (IPC): G06F011/30

ABSTRACT:

PROBLEM TO BE SOLVED: To provide a method for detecting as a WDT error the software that a routine including a WDT processing, of which is in an abnormal state.

SOLUTION: Routine identifier information DATA (4B) to (4N) of a program

12,
which is being executed at present by a CPU 1, is transmitted to a WDT monitoring unit 6 that includes a WDT counter 10 together with WDT clear instruction DATA (4A) and the WDT monitoring unit 6 compares the received
routine identifier information with the last routine identifier information in a comparison circuit 8. When both of these are different, the WDT clear instruction DATA (4A) is communicated to the WDT counter and the WDT counter is
reset and, when it is detected within a regulated time that the WDT counter is
not reset, the CPU is notified of an overflow signal 5.

US-PAT-NO: 5495102

DOCUMENT-IDENTIFIER: US 5495102 A

TITLE: Shopping cart monitoring system

DATE-ISSUED: February 27, 1996

US-CL-CURRENT: 250/222.1, 250/221 , 250/223R

APPL-NO: 08/136085

DATE FILED: October 14, 1993

---------- KWIC ---------

Detailed Description Text - DETX (60):

The watch dog timer is designed to reset the system in the event of program failure. It is a retriggerable counter which generates a reset pulse unless it is retriggered (strobed) before it times out. The following sequence is used to ensure that the main program and interrupt routines are working correctly.

Detailed Description Text - DETX (62):

If the counter is non zero, the main program strobes the watch dog timer once each time it executes a pass through its loop. This prevents the watch dog timer from resetting the system. If the interrupt routine fails, the counter is not reset to its maximum value, and eventually is decremented to 0. The main program then stops strobing the watch dog timer, and the system is reset by the watch dog timer when it times out. If the main program fails, the watch dog timer is not strobed, and once again the system is reset. If the

hardware state of the microcontroller is changed by a transient, it is returned
to normal at the start of the next loop execution when the microcontroller hardware is reinitialized.